

# Curriculum Vitae of Amir H. ASHOURI

## *Personal Data*

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**Status:** Permanent Resident (PR) of Canada  
**PEO:** Practicing Professional Engineer in Ontario (As of July 2018)  
**Webpage:** <http://www.eecg.utoronto.ca/~aashouri/>

## *Education*

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- **January 2017 –**  
**Postdoctoral Fellow**  
University of Toronto (<http://www.utoronto.ca>)  
Advisor: [Tarek Abdelrahman](#)
- **January 2013 – December 2016 (4 Years)**  
**Ph.D.** in Computer Engineering  
Polytechnic University of Milan (<http://www.polimi.it>)  
**Final Thesis:** Compiler Autotuning using Machine Learning Techniques  
(<https://www.politesi.polimi.it/handle/10589/129561>)(**Grade:** Cum laude – w/ honors)  
**Advisors:** [Cristina Silvano](#), [Gianluca Palermo](#), and [John Cavazos](#) (at Univ. Of Delaware, DE, USA)
- **September 2010 – December 2012 (2 Years)**  
**M.Sc.** in Computer Engineering  
Polytechnic University of Milan (<http://www.polimi.it>)  
**Final Thesis:** Design Space Exploration Methodology For Compiler Parameters in VLIW Processors  
(<https://www.politesi.polimi.it/handle/10589/72083>) (**Grade:** A)
- **January 2005 – Oct 2009 (4.5 years)**  
**B.Sc.** in Computer Engineering  
Iran University of Science and Technology (<http://www.iust.ac.ir>)

## *Teaching Experience* (<http://www.eecg.toronto.edu/~aashouri/-teaching>)

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- (Fall 2019) EECS4404 (Intro. To Machine Learning) & EECS2021 (Computer Organization), *York University*
- (Spring 2019) ECE421/1513 (*Introduction to Machine Learning*), *University of Toronto*
- (Spring 2014-2016) 3 editions, TA/Co-lecturing, “*Advanced Computer Architecture*”, *Polytech. Univ of Milan*
- (Spring 2014) Invited Seminars, “*Code Optimizations and Transformation*”, *Polytechnic University of Milan*

## *Research Interests*

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- Machine Learning
- Accelerating Deep Learning Applications
- Automatic Tuning
- Computer Architecture

## **Selected Publications** (*h-index: 8, Citations: 173; Full list is on [Google Scholar profile](#)*)

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- **[J4]** **A. H. Ashouri**, T. Abdelrahman, A. Dos Remedios, "*Retraining-free Methods for Fast On-the-fly Sparsification of Convolutional Neural Networks*", **Elsevier Neurocomputing**, 2019
- **[J3]** **A. H. Ashouri**, W. Killian, J. Cavazos, G. Palermo, and C. Silvano. "*A Survey on Compiler Autotuning using Machine Learning*" **ACM Transactions on Computing Survey (CSUR)** - 51, 5, Article 96 (January 2019), 42 pages
- **[W2]** **A. H. Ashouri**, T. Abdelrahman, A. Dos Remedios, "*Fast On-the-fly Retraining-free Sparsification of Convolutional Neural Networks*", **NIPS (NeurIPS) 2018 workshop** on Compact Deep Neural Networks with industrial applications (CDNNRIA), arXiv preprint arXiv:1811:04199 (2018)
- **[C4]** C. Silvano, G. Palermo, G. Agosta, **A. H. Ashouri**, D. Gadioli, et al., "*Autotuning and Adaptivity in Energy Efficient HPC Systems: The ANTAREX toolbox*", **ACM Computing Frontiers (CF)**, 2018
- **[C3]** D. Gadioli, R. Nobre, P. Pinto, E. Vitali, **A. H. Ashouri**, G. Palermo, J. Cardoso, C. Silvano, "*SOCRATES—A seamless online compiler and system runtime autotuning framework for energy-aware applications*", **IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE)**, 2018
- **[BOOK]** **A. H. Ashouri**, J. Cavazos, G. Palermo, and C. Silvano. "*Automatic Tuning of Compilers using Machine Learning Techniques*", 6 chapters, ISBN 978-3-319-71489-9, **Springer**, 2018
- **[J2]** **A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, S. Kulkarni and J. Cavazos. "*MiCOMP: Mitigating The Compiler Phase-ordering Problem using Optimization Sub-sequences and Machine Learning*" **ACM Transactions on Architecture and Code Optimization (TACO)**, 2017
- **[J1]** **A. H. Ashouri**, G. Mariani, G. Palermo, E.J. Park, J. Cavazos, and C. Silvano. "*COBAYN: Compiler Autotuning Framework Using Bayesian Networks*" **ACM Transactions on Architecture and Code Optimization (TACO)**, 2016
- **[W1]** **A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, "*Predictive Modeling Methodology for Compiler Phase-ordering*", **ACM Workshop of PARMA-DITAM co-located with HiPEAC Conference**, 2016
- **[C2]** **A. H. Ashouri**, G. Mariani, G. Palermo and C. Silvano, "*A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors*", **IEEE 12th Symposium on Embedded Systems for Real-time Multimedia (ESTIMedia)**, 2014
- **[C1]** **A. H. Ashouri**, S. Xydis, V. Zaccaria, G. Palermo and C. Silvano, "*A Framework for Compiler-level Statistical Analysis over Customized VLIW architecture*", 21st **IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)**, 2013

## **Research Experience**

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**At University of Toronto (Canada) (Advisor: *Tarek Abdelrahman*) –**  
(<http://www.eecg.toronto.edu/~tsa/>)

- (July 2019- ) Conducting research on deep learning model quantization and compression techniques
- (Jan 2017- ) Conducting research on accelerating deep learning inference for mobile and embedded devices in partnership with *Qualcomm Canada* Inc.
- (July 2017- June 2019) Conducting research on sparsification and quantization techniques for CNNs

**At High Performance Computing and Compiler lab (Supervisor: *John Cavazos*) – University of Delaware (USA) (<http://www.eecis.udel.edu/~cavazos/>)**

- (Sep 2014- March 2016) Conducting research on compiler optimization using different fine-grain kernel characterizations and utilizing machine learning for compiler auto-tuning utilizing GCC, GCC-ARM

**At System Architecture Group (Advisors: *Cristina Silvano, Gianluca Palermo*)- Polytechnic University of Milan (Italy) (<http://sagroup.elet.polimi.it/>)**

- (Sep 2015- Dec 2016) collaborating research on **ANTAREX** European Funded High-performance Computing Project ([www.antarex-project.eu](http://www.antarex-project.eu)) on Compiler Phase-ordering and Application Autotuning
- (Jan 2011- July 2015) conducting research on compiler optimization, using machine learning, Design Space Exploration and Static-Dynamic analysis and building tool-chains targeting embedded domain architectures (ARM, VLIW) utilizing compilers such as LLVM, GCC and VEX

### ***Awards and Grants***

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- (June 2017 - 2019) **Mitacs Elevate** Postdoctoral Fellowship: In collaboration with Qualcomm Inc. Canada, CAD\$ 110,000 (over 2 years)
- (July 2017- Feb 2018) **HIPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (<http://www.hipeac.net>): **Winner** of Postdoctoral grant for proposal on *using deep learning to autotune applications.*, CAD\$ 8,000
- (April 2017) Best IEEE (Italy-section) **PhD Thesis Award** of 2016 (<http://www.computersociety.it/ieee-computer-society-italy-section-chapter-2016-phd-thesis-award/>), CAD\$ 750
- (March 2016) Microsoft Student Research Competition (**SRC**): 2016, Spain, CAD\$ 750
- (Jan 2015 - Dec 2016): **Research Fellowship** by ANTAREX EU-Project in Italy, CAD\$ 20,000
- (July 2014 - Feb 2015) **HIPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (<http://www.hipeac.net>): **Winner** of PhD grant for proposal on *using machine learning for compiler phase ordering.*, CAD\$ 8,000
- (Dec 2012- Dec 2015): **PhD Fellowship** by Ministry of Science in Italy, CAD\$ 54,000 (over 3 years)

### ***Volunteerism and Service***

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- (April 2019) Artifact Evaluation Committee at **ACM LCTES 2019** (<https://lctes2019-ae.hotcrp.com/users?t=pc>)
- (July 2018) Invited Talk: "Compiler Autotuning using Machine Learning: A State-of-the-art Review", Polytechnic University of Milan (<http://www.eecg.toronto.edu/~aashouri/#activity>)
- (June 2018) Reviewer at **ACM TACO** (Transactions on Architecture and Code Optimization)
- (2018) Co-chair of Technical Committee–Professional Engineering Ontario (**PEO**) – West Toronto Chapter
- (2017 - ) Reviewer at **JCST** (Springer Journal of Computer Science and Technology)
- (2017 - ) Reviewer at **JPDC** (Elsevier Journal of Parallel and Distributed Computing)
- Subreviewer at **PACT** 2018, **ICTAI** 2016, **DSD** 2017, **ASAP** 2016-17
- Artifact Evaluation Committee at **IEEE/ACM CGO** 2018 (<https://cgo18ae.hotcrp.com/users?t=pc>)
- Student Volunteer at **HIPEAC 2016, Computing Frontiers 2016, Supercomputing (SC) 2015, FPL 2015**
- Web chair and poster-submissions *chair* at **DATE 2016** 1<sup>st</sup> workshop on REsource Awareness and Application Auto-tuning in Adaptive and heterogeNeous compuTing (**Res4Ant**) (<http://res4ant.deib.polimi.it/>)