Curriculum Vitae of

Amir H. ASHOURI

Personal Data

Status: Permanent Resident (PR) of Canada (Pending application to become a Canadian citizen)
PEO: Practicing Professional Engineer in Ontario (As of July 2018)
Website: http://amirashouri.ca

Education

- **Postdoctoral Fellowship (Jan 2017 – Dec 2019) - (3 years)**
  University of Toronto (http://www.utoronto.ca)
  Advisor: Tarek Abdelrahman
- **Ph.D**. (**Jan 2013 – Dec 2016) - (4 Years)**
  Polytechnic University of Milan (http://www.polimi.it)
  Final Thesis: Compiler Autotuning using Machine Learning Techniques (Won best IEEE Italy PhD Award - 2016) (https://www.politesi.polimi.it/handle/10589/129561)(**Grade**: Cum laude – w/ honors)
  Advisors: Cristina Silvano, Gianluca Palermo, and John Cavazos (at Univ. Of Delaware, DE, USA)
- **M. Sc**. (**Sep 2010 – Dec 2012) - (2 Years)**
  Polytechnic University of Milan (http://www.polimi.it)
  Final Thesis: Design Space Exploration Methodology For Compiler Parameters in VLIW Processors (https://www.politesi.polimi.it/handle/10589/72083) (**Grade**: A)
- **B. Sc**. (**Jan 2005 – Oct 2009) - (4.5 years)**
  Iran University of Science and Technology (http://www.iust.ac.ir)

Teaching Experience (http://amirashouri.ca/#teaching)

- (Fall/Winter 2019/20) EECS4404 (Intro. To Machine Learning)
- (Fall 2019) EECS2021 (Computer Organization), *York* University
- (Spring 2019) ECE421/1513 (*Introduction to Machine Learning)*, *University of Toronto*
- (Spring 2014-2016) 3 editions, TA/Co-lecturing, "*Advanced Computer Architecture*", *Polytech. Univ of Milan*
- (Spring 2014) Invited Seminars, "*Code Optimizations and Transformation*", *Polytechnic University of Milan*

Research/Work Experience

Senior AI-Compiler Engineer, Huawei (Canada)

- (Jan 2020 -) Collaborating on Huawei's AI-compiler infrastructure's Frontend/Midend (LLVM-based).
- (Jan 2020 -) Conducting research on Huawei's Autotuning framework leveraging Machine Learning

Postdoctoral Fellow, University of Toronto (Canada) (Advisor: *Tarek Abdelrahman*)

- (Jan 2017 - Dec 2019) Conducting research on accelerating deep learning inference for mobile and embedded devices in partnership with *Qualcomm Canada* Inc.

- (July 2017- Dec 2019) Conducting research on sparsification and quantization techniques for CNNs

Visiting Scholar, High Performance Computing and Compiler lab (Supervisor: *John Cavazos*) – University of Delaware (USA)

- (Sep 2014 - March 2016) Conducting research on compiler optimization using different fine-grain kernel characterizations and utilizing machine learning for compiler auto-tuning utilizing GCC, GCC-ARM

PhD Fellow, System Architecture Group (Advisors: *Cristina Silvano*, *Gianluca Palermo*)- Polytechnic University of Milan (Italy)

- (Sep 2015 - Dec 2016) collaborating research on ***ANTAREX*** European Funded High-performance Computing Project (www.antarex-project.eu) on Compiler Phase-ordering and Application Autotuning

- (Jan 2011- July 2015) conducting research on compiler optimizations using machine learning, Design Space Exploration (DSE), and Static-Dynamic analysis and building tool-chains targeting embedded domain architectures (ARM, VLIW) utilizing compilers such as LLVM, GCC and VEX

Research Interests

- Machine Learning
- Accelerating Deep Learning Applications
- Automatic Tuning
- Compilers

*Selected Publications (**h-index: 10**, **Citations: 322**; Full list is on **Google Scholar profile**)*

- **[J4] A. H. Ashouri**, T. Abdelrahman, A. Dos Remedios, "*Retraining-free Methods for Fast On-the-fly Sparsification of Convolutional Neural Networks*", **Elsevier Neurocomputing**, 2019

- **[J3] A. H. Ashouri**, W. Killian, J. Cavazos, G. Palermo, and C. Silvano. "*A Survey on Compiler Autotuning using Machine Learning*" ***ACM Transactions on Computing Survey (CSUR)*** - 51, 5, Article 96 (January **2019**), 42 pages

- **[W2] A. H. Ashouri**, T. Abdelrahman, A. Dos Remedios, "*Fast On-the-fly Retraining-free Sparsification of Convolutional Neural Networks*", **NIPS (NeurIPS) 2018 workshop** on Compact Deep Neural Networks with industrial applications (CDNNRIA), arXiv preprint arXiv:1811:04199 (2018)

- **[C4]** C. Silvano, G. Palermo, G. Agosta, **A. H. Ashouri**, D. Gadioli, et al., "*Autotuning and Adaptivity in Energy Efficient HPC Systems: The ANTAREX toolbox*", **ACM Computing Frontiers** *(***CF), 2018**

- **[C3]** D. Gadioli, R. Nobre, P. Pinto, E. Vitali, **A. H. Ashouri**, G. Palermo, J. Cardoso, C. Silvano, "*SOCRATES—A seamless online compiler and system runtime autotuning framework for energy-aware applications*", **IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition** *(***DATE), 2018**

- **[BOOK] A. H. Ashouri**, J. Cavazos, G. Palermo, and C. Silvano. "*Automatic Tuning of Compilers using Machine Learning Techniques*", 6 chapters, ISBN 978-3-319-71489-9**, *Springer, 2018***

- **[J2] A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, S. Kulkarni and J. Cavazos. "*MiCOMP: Mitigating The Compiler Phase-ordering Problem using Optimization Sub-sequences and Machine Learning*" ***ACM Transactions on Architecture and Code Optimization (TACO)*, 2017**

- **[J1] A. H. Ashouri**, G. Mariani, G. Palermo, E.J. Park, J. Cavazos, and C. Silvano. "*COBAYN: Compiler Autotuning Framework Using Bayesian Networks*" ***ACM Transactions on Architecture and Code Optimization (TACO)*, 2016**

- **[W1] A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, "*Predictive Modeling Methodology for Compiler Phase-ordering*", **ACM Workshop of *PARMA-DITAM co-located with HiPEAC Conference,* 2016**

- **[C2] A. H. Ashouri**, G. Mariani, G. Palermo and C. Silvano, "*A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processsors*", **IEEE 12th Symposium on Embedded Systems for Real-time Multimedia (*ESTIMedia*), 2014**

- **[C1] A. H. Ashouri**, S. Xydis, V. Zaccaria, G. Palermo and C. Silvano, "*A Framework for Compiler-level Statistical Analysis over Customized VLIW architecture*", 21st **IFIP/IEEE International Conference on Very Large Scale Integration (*VLSI-SoC*), 2013**

Awards and Grants

- (June 2017 – July 2019) ***Mitacs Elevate*** Postdoctoral Fellowship: In collaboration with Qualcomm Inc. Canada, CAD$ 110,000 (over 2 years)

- (July 2017- Feb 2018) **HiPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (http://www.hipeac.net): ***Winner*** of Postdoctoral grant for proposal on *using deep learning to autotune applications*., CAD$ 8,000

- (April 2017) Best IEEE (Italy-section) ***PhD Thesis Award*** of 2016 (http://www.computersociety.it/ieee-computer-society-italy-section-chapter-2016-phd-thesis-award/), CAD$ 750

- (March 2016) Microsoft Student Research Competition (**SRC**): 2016, Spain, CAD$ 750

- (Jan 2015 - Dec 2016): **Research Fellowship** by ANTAREX EU-Project in Italy, CAD$ 20,000

- (July 2014 - Feb 2015) **HiPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (http://www.hipeac.net): ***Winner*** of PhD grant for proposal on *using machine learning for compiler phase ordering*., CAD$ 8,000

- (Dec 2012- Dec 2015): **PhD Fellowship** by Ministry of Science in Italy, CAD$ 54,000 (over 3 years)

Volunteerism and Service

- (2020 -) **Reviewer** at ACM TECS (Transactions on Embedded Computing Systems)
- (October 2019) **Invited talk** at Google Brain (http://amirashouri.ca/#talks)
- (April 2019) **Artifact Evaluation Committee** at ACM LCTES *(https://lctes2019-ae.hotcrp.com/users?t=pc)*
- (July 2018) **Invited Talk**: Polytechnic University of Milan (http://amirashouri/#talks)
- (2018 -) **Reviewer** at ACM TACO (Transactions on Architecture and Code Optimization)
- (2018) **Co-chair** of Technical Committee–Professional Engineering Ontario (**PEO**) – West Toronto Chapter
- (Nov 2017) **Artifact Evaluation Committee** at CGO 2018 (https://cgo18ae.hotcrp.com/users?t=pc)
- (2017 -) **Reviewer** at JCST (Springer Journal of Computer Science and Technology)
- (2017 -) **Reviewer** at JPDC (Elsevier Journal of Parallel and Distributed Computing)
- (2016 - 2018) **Subreviewer** at PACT 2018, *ICTAI* 2016, DSD 2017, ASAP 2016-17
- (2015 - 16) **Student Volunteer** at *HiPEAC '16*, *Computing Frontiers '16*, *Supercomputing (SC) '15*, *FPL 2015*
- (2015) **Web chair *and* poster-submissions chair** at **DATE** 1st workshop on RESource Awareness and Application Auto-tuning in Adaptive and heterogeNeous compuTing (***Res4Ant***) (http://res4ant.deib.polimi.it/)